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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,923	12/08/2005	Yoshinari Tsukada	SHM-16366	1496

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EXAMINER	
WILLIAMS, ALEXANDER O	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/559,923	TSUKADA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-7 and 9-16* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/559923 Attorney's Docket #: SHM-16366
Filing Date: 4/23/2004: claimed foreign priority to 6/10/2003

Applicant: Tsukada et al.

Examiner: Alexander Williams

Applicant's Amendment filed 2/19/08 has been acknowledged.

Claim 4 has been cancelled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3, 5, 6, 11, 12, 13, 14 and 16 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishikawa et al. (U.S. Patent # 6,911,728 B2).

3. Ishikawa et al. (figures 1 to 16) specifically figure 15 show a semiconductor device comprising: a semiconductor element **108**; a heat sink **102**; a laminar plate **104** provided between the semiconductor element and the heat sink, said laminar plate including an intermediate layer for moderating thermal stress, wherein the laminar plate comprises a first metal plate **126**, the intermediate layer **126**, a second metal plate **116**, an insulating member **114**, and a third metal plate **112**, wherein: said first metal plate being interposed between the semiconductor element and the intermediate layer, said first metal plate having one side bonded to the semiconductor element and an opposite side bonded to a first side of the intermediate layer; said second metal plate being interposed between the intermediate layer and the insulating member, whereby one side of said second metal plate is bonded to a second, opposite side of the intermediate layer and the other side of said second metal plate is bonded to a first side of the intermediate layer; and said insulating member is interposed between the second and third metal plates, whereby said third metal plate is bonded to a second opposite side of the insulating member.

5. The semiconductor device according to claim 3, Ishikawa et al. show wherein a thickness of the second metal plate is equal to a thickness of the third metal plate.

12. The semiconductor device according to claim 3, Ishikawa et al. show wherein the insulating member **114** is formed of a material that is an electrical insulator and a thermal conductor.

13. The semiconductor device according to claim 12, Ishikawa et al. show wherein insulating member is formed of SiN.

14. The semiconductor device according to claim 3, Ishikawa et al. show wherein the first metal plate **126** further includes a nickel plating **128** on a surface of the first metal plate to which the semiconductor element **108** is mounted.

16. The semiconductor device according to claim 3, Ishikawa et al. show wherein the semiconductor element has a first side and a second side, the first metal plate has a first side and a second side, and the intermediate layer has a first side and a second side, wherein, the semiconductor element second side is directly bonded to the first side of the metal plate, and the second side of the metal plate is directly bonded to the first side of the intermediate layer.

Claims 1-3, 5-7 and 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arakawa et al. (U.S. Patent # 4,497,875) in view of Ishikawa et al. (U.S. Patent # 6,911,728 B2).

1. Arakawa et al. (figures 1 to 4) specifically figure 4 show a semiconductor device comprising: a semiconductor element **731**; a first metal layer **63** bonded **(bonded by layers between 731 and 63)** to one side of the semiconductor element; an intermediate layer **23** bonded **(bonded directly)** to one side of the first metal layer remote from the semiconductor element, the intermediate layer being made of a carbon-copper composite material; a second metal layer **33** bonded **(bonded directly)** to one side of the intermediate layer remote from the first metal layer; an insulating member **1** bonded **(bonded directly)** to one side of the second metal layer remote from the intermediate layer; and a third metal layer **4** bonded **(bonded directly)** to one side of the insulating member remote from the second metal layer, the third metal layer having a thickness substantially equal to that of the second metal layer; and, a heat sink **5**; wherein the first, second and third metal layers are made of a same material **(all made from at least the same material of copper)**. Arakawa et al. fail to explicitly show plates. However, Arakawa et al. does disclose metal layers.

3. Arakawa et al. (figures 1 to 4) specifically figure 4 show a semiconductor device comprising: a semiconductor element **731**; a heat sink **5**; a laminar layer **63,23,33,1,4** provided between the semiconductor element and the heat sink, said laminar layer including an intermediate layer for moderating thermal stress, wherein the laminar layer comprises a first metal layer **63**, the intermediate layer **23**, a second metal layer **33**, an insulating member **1**, and a third metal layer **4**, wherein: said first metal layer being interposed between the semiconductor element **731** and the intermediate layer **23**, said first metal layer **63** having one

side bonded **(bonded by the layers between 731 and 23)** to the semiconductor element and an opposite side bonded **(directly bonded)** to a first side of the intermediate layer; said second metal layer **33** being interposed between the intermediate layer **23** and the insulating member **1**, whereby one side of said second metal layer **33** is bonded to a second, opposite side of the intermediate layer **23** and the other side of said second metal plate **33** is bonded to a first side of the intermediate layer **23**; and said insulating member **1** is interposed between the second **33** and third **4** metal layers, whereby said third metal layer **4** is bonded to a second opposite side of the insulating member **1**. Arakawa et al. fail to explicitly show plates. However, Arakawa et al. does disclose metal layers.

FIG. 4 shows an example of a hybrid integrated circuit device incorporating a ceramics substrate with metal plate in accordance with an embodiment of the invention, in which the same reference numerals are used to denote the same parts or members as those used in the embodiment shown in FIG. 3. The hybrid integrated circuit device has an insulation plate 1 made from alumina and a plurality of metal plates 21, 22, 23 and 24 fuctioning as lead plates and made of copper-carbon fibers composite material and bonded to one side of the insulation plate 1 through respective brazing layers 31, 32, 33 and 34 made from Cu.sub.2 O--Cu or CuO--Cu. To the other side of the insulation plate 1, bonded through a brazing layer 4 consisting of Cu.sub.2 O--Cu or CuO--Cu is a metal plate 5 functioning as a heat radiating plate and made of a copper-carbon fibers composite material. Reference numerals 61, 62, 63 and 64 denote copper films coated on the upper surfaces of the metal plates 21, 22, 23 and 24. A semiconductor element 71 consisting of a semiconductor pellet 711 and ohmic contacts 712 and 713 is placed on the metal plate 21. Similarly, a semiconductor element 73 consisting of a semiconductor pellet 731 and ohmic contacts 732, 733 and 734 is placed on the metal plate 23. Numerals 81 and 83 denote brazing layers. The numerals 91, 92 and 93 designate bonding wires which are connected, respectively, between the ohmic contact 712 and the copper

coating film 62, between the ohmic contact 732 and the copper coating film 62 and between the ohmic contact 733 and the copper coating film 64. The copper coating films 61, 62, 63 and 64 are intended for improving the wettability of the metal plates 21, 22, 23 and 24 to the solder and for improving the bonding ability of the metal plates 21, 22, 23 and 24 to the bonding wires 91, 92 and 93. These copper coating films may be formed by bonding copper foils simultaneously with when forming the copper-carbon fibers composite material by hot press. By so doing, it is possible to simplify the production process.

Ishikawa et al. is cited for showing an electronic circuit. Specifically, Ishikawa et al. (figures 1 to 16) specifically figure 15 show a semiconductor device comprising: a semiconductor element **108**; a heat sink **102**; a laminar plate **104** provided between the semiconductor element and the heat sink, said laminar plate including an intermediate layer for moderating thermal stress, wherein the laminar plate comprises a first metal plate **126**, the intermediate layer **126**, a second metal plate **116**, an insulating member **114**, and a third metal plate **112**, wherein: said first metal plate being interposed between the semiconductor element and the intermediate layer, said first metal plate having one side bonded to the semiconductor element and an opposite side bonded to a first side of the intermediate layer; said second metal plate being interposed between the intermediate layer and the insulating member, whereby one side of said second metal plate is bonded to a second, opposite side of the intermediate layer and the other side of said second metal plate is bonded to a first side of the intermediate layer; and said insulating member is interposed between the second and third metal plates, whereby said third metal plate is bonded to a second opposite side of the insulating member for the purpose of protecting semiconductors devices against a thermal breakdown.

2. The semiconductor device according to claim 1, Arakawa et al. show wherein the intermediate layer is adapted to moderate thermal stress.

5. The semiconductor device according to claim 4, the combination with Arakawa et al. show wherein a thickness of the second metal plate is equal to a thickness of the third metal plate.

6. The semiconductor device according to claim 3, the combination with Arakawa et al. show wherein the intermediate layer for moderating thermal stress comprises a carbon-copper composite material.

7. The semiconductor device according to claim 1, the combination with Ishikawa et al. show wherein the first metal plate **126** further includes a nickel plating **128** on a surface of the first metal plate to which the semiconductor element **108** is mounted.

9. The semiconductor device according to claim 1, the combination with Ishikawa et al. show wherein the insulating member **114** is formed of a material that is an electrical insulator and a thermal conductor.

10. The semiconductor device according to claim 9, the combination with Ishikawa et al. show wherein insulating member is formed of SiN.

12. The semiconductor device according to claim 3, the combination with Ishikawa et al. show wherein the insulating member **114** is formed of a material that is an electrical insulator and a thermal conductor.

13. The semiconductor device according to claim 12, the combination with Ishikawa et al. show wherein insulating member is formed of SiN.

14. The semiconductor device according to claim 3, the combination with Ishikawa et al. show wherein the first metal plate **126** further includes a nickel plating **128** on a surface of the first metal plate to which the semiconductor element **108** is mounted.

15. The semiconductor device according to claim 1, the combination with Ishikawa et al. show wherein the semiconductor element has a first side and a second side, the first metal plate has a first side and a second side, and the intermediate layer has a first side and a second side, wherein, the semiconductor element second side is directly bonded to the first side of the metal plate, and the second side of the metal plate is directly bonded to the first side of the intermediate layer.

16. The semiconductor device according to claim 3, the combination with Ishikawa et al. show wherein the semiconductor element has a first side and a second side, the first metal plate has a first side and a second side, and the intermediate layer has a first side and a second side, wherein, the semiconductor element second side is directly bonded to the first side of the metal plate, and the second side of the metal plate is directly bonded to the first side of the intermediate layer.

Therefore, it would be obvious to one of ordinary skill in the art to use Ishikawa et al.'s metal plates to modify Arakawa et al.'s metal layers for the purpose of protecting semiconductors devices against a thermal breakdown.

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response

Applicant's arguments filed 2/19/08 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AOW/
6/6/08

/Alexander O Williams/

Primary Examiner, Art Unit 2826